Course Code: 19EC0401 **R19**

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QUESTION BANK (DESCRIPTIVE)

Subject with Code : STLD(19EC401) **Course & Branch**: B.Tech - EEE

Year & Sem: II-B.Tech & II-Sem

UNIT –I

BINARY SYSTEMS

1. Explain about Logic gates. with symbols and truth tables. **L1, CO.1,[12M]**
2. Perform the following
   a) Subtraction by using 1's complement for the given 10101 - 11011. **L3, CO.1,[6M]**
   b) Subtraction by using 2's complement for the given 111001-1010. **L3, CO.1,[6M]**
3. a) Convert the following numbers to Decimal and then to Octal. (i) $(423416)_{10}$ (ii)$(10010011)_2$. **L1, CO.1,[6M]**
   b) Convert the following to Decimal and then to Hexadecimal. (i) $(1234)_8$ (ii) $(11001111)_2$ **L1, CO.1,[6M]**
4. Simplify the following Boolean expression:
   (a) F = (A+B)(A'+C)(B+C). **L3, CO.2,[6M]**
   (b) F = XY+XYZ+XYZ'+X'YZ **L3, CO.2,[6M]**
5. Explain Different Types of binary codes and give there examples **L3, CO.1,[12M]**
6. Convert the following to Decimal and then to Octal. **L1,CO.1,[12M]**
   (a) 1234_{16} (b) $12EF_{16}$ (c) 10110011_2 (d) 10001111_2 (e) 352_{10}
7. Express the function Y=A+B'C in (i)Canonical SOP form (ii) Canonical POS form **L3,CO.2,[12M]**

8 a) Simplify the following Boolean functions to minimum number of literals **L3, CO.2,[6M]**
   (i) xyz + x'y + xyz'. (ii) xz + x'yz.
   b) Simplify the following Boolean functions to minimum number of literals: **L3, CO.2,[6M]**
   F = ABC + ABC' + A'B

9. A receiver with even parity hamming code is received the data as 1110110.Determine the correct code. **L3,CO.2,[12M]**
10. What is Grey code? What are the rules to construct gray code? Develop the 4 bit gray code for The decimal 0 to 15. **L1, CO.1,[12M]**

UNIT –II

GATE–LEVELMINIMIZATION

1. Minimize the following Boolean function using K-Map. **L2, CO.3,[12M]**
   F(A, B, C, D)= Σm(0, 2, 4, 6, 8, 10, 12, 14).
2. Minimize the given Boolean function F(A,B,C,D) = Σ m(2,3,5,7,8,10,12,13) using tabulation method. **L2, CO.3,[12M]**
3. Simplify the following Boolean expressions using K-map and Implement the same using Logic gates. F(W,X,Y,Z)= XZ+W'XY'+WXY+W'YZ+WY'Z **L3, CO.3,[12M]**
4. Simplify the following Boolean expressions using K-map. **L3, CO.3,[12M]**
   F(A, B, C, D)= Σm(5,6,7,12,13)+ Σd(4,9,14,15)
5. a) Simplify the following expression using the K-map for the 3-variable. **L3, CO.3,[6M]**
   Y = AB'C+A'BC+A'B'C+A'B'C'+AB'C'
   b) Simplify the following Boolean expressions using K-map.
   F(A, B, C, D)= Σm(1,3,7,11,15)+ Σd(0,2,5) **L3, CO.3,[6M]**
6. Minimize the given Boolean function F(A,B,C,D) = Σ m(0,2,3,6,7,8,10,12,13) using tabulation method. **L2, CO.3,[12M]**
7. What are the universal gates? Implement logic gates by using NAND and NOR gates. **L2, CO.3,[12M]**
8. Simplify the following Boolean expressions using K-map. **L3, CO.3,[12M]**
   F(A, B, C, D)= πM(0,2,3,8,9,12,13,15)
9. Simplify the following Boolean expressions using K-map. **L3, CO.3,[12M]**
   F(A, B, C, D,E)= Σm(0,2,4,6,9,11,13,15,17,21,25,27,29,31)
10. Simplify the following Boolean expressions using K-map. **L3, CO.3,[12M]**
    F(A, B, C, D,E)= Σm(0,5,6,8,9,10,11,16,20,24,25,26,27,29,31)

UNIT –III

COMBINATIONAL LOGIC

1 Design 32:1 Mux using two 16:1 Muxs and one 2:1 Mux. **L5 CO.4,[12M]**

2 What is combinational logic circuit? Give the analysis procedure for combinational logic circuit. **L5 CO.4,[12M]**

3. Design & implement Half Adder and Full Adder with truth table. **L3 CO.4,[12M]**

4. Design & implement Half Subtractor and Full Subtractor with truth table**.** **L3 CO.4,[12M]**

5.What is magnitude comparator? Design 2-bit comparator by using logic gates. **L1,CO.4,[12M]**

6.What is parallel adder? Design and explain 4 bit parallel adder by using full adder. **L3, CO.4,[12M]**

7.What is Decoder? Design the circuit for 3to 8 decoder with truth table. **L1,CO.4,[12M]**

8. What is Encoder? Design the circuit for Octal to Binary encoder with truth table. **L1,CO.4,[12M]**

9. Design 32 to1 multiplexer using 8 to 1 multiplexers and 2to4 Decoder. **L1,CO.4,[12M]**

10.What is Demultiplexer? Desingn1:8 Demultiplexer using 1:4 Demultiplexers. **L1,CO.4,[12M]**

UNIT-IV
SYNCHRONOUS SEQUENTIAL LOGIC

1. a) Draw the logic diagram for D Flip Flop by using SR Flip Flop Explain the operation with truth table. **L1, CO.4[7M]**
   b) Write the differences between combinational and sequential circuits. **L2, CO.4[5M]**
2. a) Explain working of Master Slave Flip flop with neat diagram. **L1, CO.4,[6M]**
   b)Draw the logic diagram T Flip Flop by using JK Flip Flop and draw the timing diagram. **L1, CO.2,[6M]**
3. Draw the circuit of JK flip flop using NAND gates and explain its operation. **L3,CO.4,[12M]**
4. What is SR latch? Explain the operation for different cases By using Truth table. **L1,CO.4,[12M]**
5. What is Register Explain i) Parallel in Parallel out Register **L3,CO.4,[12M]**
   ii) Series in Parallel out Register
6. Design and implement 3-bit ripple counter using J-K flip flop. Draw the state diagram, logic diagram and timing diagram for the same. **L3,CO.4,[12M]**
7. With a neat sketch explain 4 bit Johnson counter using D FF. **L3,CO.4,[12M]**
8. Implement 4-bit ring counter using suitable shift register. Briefly describe its operation. **L3,CO.4,[12M]**
9. a) Explain about level and Edge triggering . **L1,CO.4,[6M]**
   b)Explain the operation of series in series out register. **L1, CO.4,[6M]**
10. Design MOD-10 Asynchronous counter by using T-Flip flop **L3, CO.4,[12M]**

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UNIT –V
FINITE STATE MACHINES AND PROGRAMMABLE LOGIC DEVICES

1. Explain about Mealy and Moore Models of sequential machines. **L3, CO.5,[12M]**
2. Implement the following Boolean function using PAL. **L3, CO.6,[12M]**

   (i)W(A,B,C,D) = Σm(0,2,6,7,8,9,12,13) (ii)X(A,B,C,D) = Σm(0,2,6,7,8,9,12,13,14)
   (iii)Y(A,B,C,D) = Σm(2,3,8,9,10,12,13) (iv)Z(A,B,C,D) = Σm(1,3,4,6,9,12,14)
3. What is design procedure for FSM? Give the advantages of FSM. **L3, CO.5,[12M]**
4. Implement PLA circuit for the following functions F1(A,B,C)= Σm(3,5,6,7),

   F2(A,B,C)= Σm(0,2,4,7). **L3, CO.6,[12M]**
5. Given the 8-bit data word 01011011,generate the 12-bit composite word for the hamming code that corrects and detects single errors. **L1, CO.6,[12M]**
6. Explain the following related to sequential circuits.
   a)State diagram.
   b) State table.
   c) State assignment. **L2, CO.6,[12M]**
7. What is ROM organization? Explain about Different types of ROM. **L3, CO.6,[12M]**
8. Compare three combinational circuits: PLA, PAL and PROM. **L3, CO.6,[12M]**

9.a) What is FSM? Give the applications of FSM. **L3, CO.5,[6M]**

b) Explain about Memory decoding. **L3, CO.6,[6M]**

10.What is RAM organization? Explain about Different types of RAM. **L3, CO.6,[12M]**

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